



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,938	03/15/2004	G. Glenn Henry	CNTR.2072	1288

23669 7590 08/20/2007  
HUFFMAN LAW GROUP, P.C.  
1900 MESA AVE.  
COLORADO SPRINGS, CO 80906

EXAMINER
----------

LANIER, BENJAMIN E

ART UNIT	PAPER NUMBER
----------	--------------

2132

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/20/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO@HUFFMANLAW.NET

<b>Office Action Summary</b>	<b>Application No.</b> 10/800,938	<b>Applicant(s)</b> HENRY ET AL.	
	<b>Examiner</b> Benjamin E. Lanier	<b>Art Unit</b> 2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                 | 5) <input type="checkbox"/> Notice of Informal Patent Application                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

**DETAILED ACTION*****Double Patenting***

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 56, 59, 66, 84, 87, 94 of Application No. 10/674,057 contain(s) every element of claims 21, 22, 25 of the instant application and as such are not patentably distinct from an earlier patent claim(s).

3. Claims 1-3, 9-18, 25, 28-30 of Application No. 10/826,435 contain(s) every element of claims 1-4, 7-15, 21, 22, 25 of the instant application and as such are not patentably distinct from an earlier patent claim(s).

4. Claims 1-4, 20-29, 40, 50-52 of Application No. 10/727,973 contain(s) every element of claims 1-4, 7-15, 21, 22, 25 of the instant application and as such are not patentably distinct from an earlier patent claim(s).

Art Unit: 2132

“A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus).” ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

“Claim 12 and Claim 13 are generic to the species of invention covered by claim 3 of the patent. Thus, the generic invention is “anticipated” by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim). This court’s predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller, 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 12 and 13 were properly rejected under the doctrine of obviousness-type double patenting” (In re Goodman (CA FC) 29 USPQ2d 2010 (12/3/1993)).

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2132

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6, 8-19, 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Kessler, U.S. Patent No. 6,789,147. Referring to claims 1, 21, Kessler discloses a co-processor that includes multiple execution units (Figure 2) wherein each of the execution units includes an execution queue to store cryptographic instructions received by the co-processor (Figure 8), which meets the limitation of a cryptographic instruction, received by a computing device as a part of an instruction flow executing on said computing device, wherein said cryptographic instruction prescribes one of the cryptographic operations. The execution units include a plurality of operation blocks that correspond to different cryptographic operations that are used depending upon the type of instruction received in the execution queue (Figure 8 & Col. 9, lines 7-43), which meets the limitation of wherein said cryptographic instruction prescribes one of a plurality of cryptographic algorithms, algorithm logic, operatively coupled to said cryptographic instruction, configured to direct said computing device to execute said one of the cryptographic operations according to said one of a plurality of cryptographic algorithms. Using the appropriate operation block, the corresponding cryptographic algorithm is used when processing the received instruction (Col. 9, lines 28-43), which meets the limitation of execution logic, operatively coupled to said algorithm logic, configured to execute said one of the cryptographic operations.

Referring to claims 2, 3, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as AES, 3DES, DES, and RC4 (Figures 5 & 8), which meets the limitation of an encryption operation, said encryption operation comprises encryption of a plurality of plaintext blocks to generate a corresponding plurality of ciphertext blocks, a

decryption operation, said decryption operation comprising decryption of a plurality of ciphertext blocks to generate a corresponding plurality of plaintext blocks.

Referring to claims 4, 22, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as AES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Advanced Encryption Standard (AES) algorithm.

Referring to claims 5, 23, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as DES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Digital Encryption Standard (DES) algorithm.

Referring to claims 6, 24, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as 3DES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Triple-DES algorithm.

Referring to claims 8, 9, Kessler discloses that each execution unit includes a register file block that includes that data to be operated on by the corresponding cryptographic algorithm (Figure 8 & Co. 9, lines 18-40), which meets the limitation of said cryptographic instruction implicitly references a plurality of registers within said computing device, a first register, wherein contents of said first register comprise a first pointer to a first memory address, said first memory address specifying a first location in memory for access of said plurality of input text blocks upon which said one of the cryptographic operations is to be accomplished.

Referring to claim 10, Kessler discloses that each execution unit includes a register file block that includes that data to be operated on by the corresponding cryptographic algorithm

Art Unit: 2132

(Figure 8 & Co. 9, lines 18-40), which meets the limitation of a second register, wherein contents of said second register comprise a second pointer to a second memory address, said second memory address specifying a second location in said memory for storage of a corresponding plurality of output text blocks, said corresponding plurality of output text blocks being generated as a result of accomplishing said one of the cryptographic operations upon a plurality of input text blocks.

Referring to claim 11, Kessler discloses that each execution unit includes a register file block that includes that data to be operated on by the corresponding cryptographic algorithm (Figure 8 & Co. 9, lines 18-40), which meets the limitation of a third register, wherein contents of said third register indicate a number of text blocks within a plurality of input text blocks.

Referring to claim 12, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as AES, 3DES, DES, and RC4 (Figures 5 & 8), which meets the limitation of a fourth register, wherein contents of said fourth register comprise a third pointer to a third memory address, said third memory address specifying a third location in memory for access of cryptographic key data for use in accomplishing said one of the cryptographic operations.

Referring to claim 13, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as RC4 (Figures 5 & 8), which meets the limitation of a fifth register, wherein contents of said fifth register comprises a fourth pointer to a fourth memory address, said fourth memory address specifying a fourth location in memory, said fourth location comprising said initialization vector location, contents of said initialization vector comprising an

Art Unit: 2132

initialization vector or initialization vector equivalent for use in accomplishing said one of the cryptographic operations.

Referring to claim 14, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as AES, 3DES, DES, and RC4 (Figures 5 & 8), which meets the limitation of a sixth register, wherein contents of said sixth register comprises a fifth pointer to a fifth memory address, said fifth memory address specifying a fifth location in memory for access of a control word for use in accomplishing said one of the cryptographic operations, wherein said control word prescribes cryptographic parameters for said one of the cryptographic operations because Applicant's specification essentially states that the control word identifies the algorithm (Page 38, paragraph 55).

Referring to claim 15, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as 3DES, DES (Figures 5 & 8), which meets the limitation of a cryptographic unit, configured execute a plurality of cryptographic rounds on each of said plurality of input text blocks to generate a corresponding each of a plurality of output text blocks, wherein said plurality of cryptographic rounds are prescribed by a control word that is provided to said cryptographic unit.

Referring to claim 16, Kessler discloses a co-processor that includes multiple execution units (Figure 2) wherein each of the execution units includes an execution queue to store cryptographic instructions received by the co-processor (Figure 8), which meets the limitation of a cryptographic unit within a device, configured to execute one of the cryptographic operations response to receipt of a cryptographic instruction within an instruction flow that prescribes said one of the cryptographic operations. The execution units include a plurality of operation blocks



Art Unit: 2132

that correspond to different cryptographic operations that are used depending upon the type of instruction received in the execution queue (Figure 8 & Col. 9, lines 7-43), which meets the limitation of an algorithm field, configured to prescribed one of a plurality of cryptographic algorithms to be employed when executing said one of the cryptographic operations. Using the appropriate operation block, the corresponding cryptographic algorithm is used when processing the received instruction (Col. 9, lines 28-43), which meets the limitation of algorithm logic, operatively coupled to said cryptography unit, configured to direct said device to perform said one of the cryptographic operations according to said one of the plurality of cryptographic algorithms.

Referring to claim 17, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as AES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Advanced Encryption Standard (AES) algorithm.

Referring to claim 18, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as DES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Digital Encryption Standard (DES) algorithm.

Referring to claim 19, Kessler discloses that the operation blocks correspond to cryptographic algorithms such as 3DES (Figures 5 & 8), which meets the limitation of one of a plurality of cryptographic algorithms comprises the Triple-DES algorithm.

***Claim Rejections - 35 USC § 103***

Art Unit: 2132

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 7, 20, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kessler, U.S. Patent No. 6,789,147, in view of Miller, U.S. Patent No. 6,081,884. Referring to claims 7, 20, 25, Kessler does not specify that the co-processor utilizes the x86 instruction set. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the co-processor described in Kessler to implement the x86 instruction set because the x86 instruction set has been widely accepted because of its compatibility with a large amount of software as taught by Miller (Col. 2, lines 9-14).

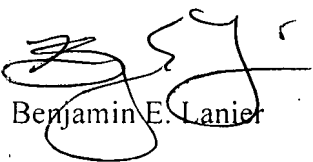
#### *Conclusion*

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin E. Lanier whose telephone number is 571-272-3805. The examiner can normally be reached on M-Th 7:30am-5:00pm, F 7:30am-4pm.

Art Unit: 2132

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Benjamin E. Lanier